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Magnetics, IEEE Transactions on , Volume: 31 Issue: 3 , May 1995

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Solid-State Circuits, IEEE Journal of , Volume: 35 Issue: 3 , March

2000

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5 A reconfigurable content addressable memory*McAuley, A.J.; Cotton, C.J.;*Custom Integrated Circuits Conference, 1990., Proceedings of the
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**6 A parallel architecture for multilevel decision feedback
equalization***Kenney, J.G.; Melas, C.M.;*

Magnetics, IEEE Transactions on , Volume: 34 Issue: 2 , March 1998

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1 Mondrian memory protection

Emmett Witchel, Josh Cates, Krste Asanovi?

October 2002 Tenth international conference on architectural support for programming
Proceedings of the 10th international conference on architectural support
operating systems (ASPLOS-X), Volume 37 , 30 , 36 Issue 10 , 5 , 5

Full text available: pdf(1.53 MB)

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Mondrian memory protection (MMP) is a fine-grained protection scheme that allows
share memory and export protected services. In contrast to earlier page-based schemes,
control at the granularity of individual words. We use a compressed permissions
and employ two levels of permissions caching to reduce run-time overheads. The protocol
less than 9% overhead to ...

2 Cache Memories

Alan Jay Smith

September 1982 ACM Computing Surveys (CSUR), Volume 14 Issue 3

Full text available: pdf(4.61 MB) Additional Information: full citation, references, citations, index terms

3 External memory algorithms and data structures: dealing with massive data

Jeffrey Scott Vitter

June 2001

ACM Computing Surveys (CSUR), Volume 33 Issue 2

Full text available:  pdf(828.46 KB)

Additional Information: full citation, abstract, references, citi


Data sets in large applications are often too massive to fit completely inside the c input/output communication (or I/O) between fast internal memory and slower e: major performance bottleneck. In this article we survey the state of the art in the (or EM) algorithms and data structures, where the goal is to exploit locality in orc varie ...

Keywords: B-tree, I/O, batched, block, disk, dynamic, extendible hashing, extern multidimensional access methods, multilevel memory, online, out-of-core, secon

4 Fine-grain access control for distributed shared memory

Ioannis Schoinas, Babak Falsafi, Alvin R. Lebeck, Steven K. Reinhardt, James R. La

November 1994 Proceedings of the sixth international conference on Architectural sup operating systems, Volume 29 , 28 Issue 11 , 5

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This paper discusses implementations of fine-grain memory access control, which cache-block-sized memory regions. Fine-grain access control forms the basis of e This paper focuses on low-cost implementations that require little or no additiona efficient implementation of shared memory on a wide range of parallel systems, t with a portability ...

5 Distributed file systems: concepts and examples

Eliezer Levy, Abraham Silberschatz

December 1990

ACM Computing Surveys (CSUR), Volume 22 Issue 4

Full text available:  pdf(5.33 MB)

Additional Information: full citation, abstract, references, citings

The purpose of a distributed file system (DFS) is to allow users of physically distr storage resources by using a common file system. A typical configuration for a DI mainframes connected by a local area network (LAN). A DFS is implemented as p connected computers. This paper establishes a viewpoint that emphasizes the dis both data and con ...

6 Efficient (stack) algorithms for analysis of write-back and sector memories

James G. Thompson, Alan Jay Smith

January 1989


ACM Transactions on Computer Systems (TOCS), Volume 7 Issu

Full text available:  pdf(2.93 MB)

Additional Information: full citation, abstract, references, citings

For the class of replacement algorithms known as stack algorithms, existing anal memory miss ratios for all memory sizes simultaneously in one pass over a memi of computations possible by this methodology in two ways. First, we show how to write-back caches. The key observation here is that a given block is clean for all i

- 7 The duality of memory and communication in the implementation of a multiprocessor
M. Young, A. Tevanian, R. Rashid, D. Golub, J. Eppinger
November 1987 ACM SIGOPS Operating Systems Review , Proceedings of the eleventh annual ACM symposium on operating systems principles, Volume 21 Issue 5

Full text available:  pdf(1.26 MB)

Additional Information: full citation, abstract, references, citations

Mach is a multiprocessor operating system being implemented at Carnegie-Mellon University. The Mach design is the use of memory objects which can be managed either by the kernel or by the user through a message interface. This feature allows applications such as transaction management, secondary storage management and page replacement. This paper explains the implementation of Mach and its ...

- 8 Session S4.1: power in memory and network processors: Embedded cache buffer support for power and performance flexibility
Afzal Malik, Bill Moyer, Roger Zhou
October 2002 Proceedings of the international conference on Compilers, architecture, and networking


Full text available:  pdf(122.19 KB)

Additional Information: full citation, abstract, references

Next generation portable devices are placing stringent requirements on overall system performance. Recognition, streaming video and high speed wireless internet access are just some of the requirements for these handheld electronic gadgets. The M2CORE M341-S processor has been designed to support sensitive portable products as well as for high end embedded control applications over the M2CORE M2 and M310 families ...

Keywords: cache control, cache management, copyback, programmable, push buffer

- 9 Efficient strategies for software-only protocols in shared-memory multiprocessors
Håkan Grahn, Per Stenström
May 1995 ACM SIGARCH Computer Architecture News , Proceedings of the 22nd annual ACM symposium on computer architecture, Volume 23 Issue 2

Full text available:  pdf(1.31 MB)

Additional Information: full citation, abstract, references, citations

The cost, complexity, and inflexibility of hardware-based directory protocols motivate the study of the implications of protocols that emulate directory management using software handlers on multiprocessors. An important performance limitation of such software-only protocols is that directory management ends up on the critical memory access path for read misses, which may prevent that support efficient data transfers ...

10 Separating data and control transfer in distributed operating systems

Chandramohan A. Thekkath, Henry M. Levy, Edward D. Lazowska

November 1994 Proceedings of the sixth international conference on Architectural support for distributed operating systems, Volume 29 , 28 Issue 11 , 5

Full text available:  pdf(1.42 MB)

Additional Information: full citation, abstract, references, citations

Advances in processor architecture and technology have resulted in workstations and local-area networks such as ATM promise a ten- to hundred-fold increase in throughput, scalability, and greatly increased reliability, when compared to current LANs. Such network and processor technologies will permit tighter coupling of distributed systems.

11 The integration of virtual memory management and interprocess communication

Robert Fitzgerald, Richard F. Rashid

May 1986 ACM Transactions on Computer Systems (TOCS), Volume 4 Issue 2

Full text available:  pdf(2.45 MB)

Additional Information: full citation, abstract, references, citations

The integration of virtual memory management and interprocess communication kernel is examined. The design and implementation of the Accent memory management performance, both on a series of message-oriented benchmarks and in normal operation.

12 Efficient PRAM simulation on a distributed memory machine

Richard M. Karp, Michael Luby, Friedhelm Meyer auf der Heide

July 1992 Proceedings of the twenty-fourth annual ACM symposium on Theory of Computing

Full text available:  pdf(815.15 KB)

Additional Information: full citation, abstract, references, citations

We present a randomized simulation of a $n \log \log(n) \log(n)$ -processor shared memory PRAM with expected delay $O(\log \log(n))$ per step of simulation. The time bound for the delay is with high probability. The algorithm is based on hashing and uses a novel simulation scheme. The simpler scheme based on hashing and have much larger expected delay: $\Theta(n \log \log(n))$.

13 Analytic evaluation of shared-memory systems with ILP processors

Daniel J. Sorin, Vijay S. Pai, Sarita V. Adve, Mary K. Vernon, David A. Wood

April 1998 ACM SIGARCH Computer Architecture News , Proceedings of the 25th annual ACM symposium on Computer architecture, Volume 26 Issue 3

Full text available:  pdf(1.45 MB)

Additional Information: full citation, abstract, references, citations

This paper develops and validates an analytical model for evaluating various types of shared-memory systems with processors that aggressively exploit instruction-level parallelism. The analytical model is many orders of magnitude faster to solve, yielding highly accurate results in seconds. The model input parameters characterize the ability of an application to exploit parallelism as well as the interaction between the application and the hardware.

14 Improving the efficiency of UNIX buffer caches

A. Braunstein, M. Riley, J. Wilkes

November 1989 ACM SIGOPS Operating Systems Review , Proceedings of the twelfth principles, Volume 23 Issue 5

Full text available:  pdf(1.46 MB)

Additional Information: full citation, abstract, references

This paper reports on the effects of using hardware virtual memory assists in main controlled experimental environment was constructed from two systems whose o (XMF) used the virtual memory hardware to assist file buffer cache search and re performance characterizations was used to study the effects of varying the buffer MB); I/O transfer sizes (from ...

15 Memory-efficient state lookups with fast updates

Sandeep Sikka, George Varghese

August 2000 ACM SIGCOMM Computer Communication Review , Proceedings of the c Architectures, and Protocols for Computer Communication, Volume 30

Full text available:  pdf(384.82 KB)

Additional Information: full citation, abstract, reference

Routers must do a best matching prefix lookup for every packet; solutions for Gig link speeds higher, we seek a scalable solution whose speed scales with memory databases. In this paper we show that providing such a solution requires careful ; pipelining. This is because fast lookups require on-chip or off-chip SRAM which is

16 Distributed operating systems

Andrew S. Tanenbaum, Robbert Van Renesse

December 1985 ACM Computing Surveys (CSUR), Volume 17 Issue 4

Full text available:  pdf(5.49 MB)

Additional Information: full citation, abstract, references, citations,

Distributed operating systems have many aspects in common with centralized on This paper is intended as an introduction to distributed operating systems, and es about them. After a discussion of what constitutes a distributed operating system computer network, various key design issues are discussed. Then several exampl examined in some detail ...

17 An efficient I/O interface for optical disks

Jeffrey S. Vitter

June 1985 ACM Transactions on Database Systems (TODS), Volume 10 Issue :

Full text available:  pdf(2.55 MB)

Additional Information: full citation, abstract, references, citations,


We introduce the notion of an I/O interface for optical digital (write-once) disks, v research. The purpose of an I/O interface is to allow existing operating systems a magnetic disks to use optical disks instead, with minimal change. We define what disk-efficient. We demonstrate a practical disk- efficient I/O interface and show tl optimum, up to a ...

18 Query evaluation techniques for large databases

Goetz Graefe

June 1993

ACM Computing Surveys (CSUR), Volume 25 Issue 2

Full text available:  pdf(9.37 MB)

Additional Information: full citation, abstract, references, citings,


Database management systems will continue to manage large data volumes. Thus manipulating large sets and sequences will be required to provide acceptable performance and extensible database systems will not solve this problem. On the contrary, the problem: In order to manipulate large sets of complex objects as efficiently as to simple records, query-processing ...

Keywords: complex query evaluation plans, dynamic query evaluation plans, extensible object-oriented database systems, operator model of parallelization, parallel algorithm set-matching algorithms, sort-hash duality

19 Architectural support for scalable speculative parallelization in shared-memory

Marcelo Cintra, José F. Martínez, Josep Torrellas

May 2000 ACM SIGARCH Computer Architecture News , Proceedings of the 27th annual architecture, Volume 28 Issue 2

Full text available:  pdf(253.29 KB)


Additional Information: full citation, abstract, references, citings,

Speculative parallelization aggressively executes in parallel codes that cannot be proposed by hardware schemes have mostly focused on single-chip multiprocessing necessarily limited by their small size. Very few schemes have attempted this technique in shared-memory systems. In this paper, we present and evaluate a new hardware parallelization. This design ...

20 Machine-independent virtual memory management for paged uniprocessor architectures

Richard Rashid, Avadis Tevanian, Michael Young, David Golub, Robert Baron

October 1987 Proceedings of the second international conference on Architectural support for operating systems, Volume 15 , 22 , 21 Issue 5 , 10 , 4

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From: atarihq.com/danb/files/mamedrv1.txt**CmpSci 535 Lecture 9**...output data directly from **memory**. Because the mameory **contains** stale ... **table** entry and if there is a mtch and the type of access (**read** vs.
From: www.cs.umass.edu/~weems/CmpSci535/535lecture9.html**JCN: A netbooting Linux system not dependent on a read/write NFS**Linux system not dependent on a **read/write** NFS ... small amounts of **memory**, /local **contains** a ... simply compares PCI ids to a **lookup table** and spits...
From: www-jcsu.jesus.cam.ac.uk/jcn/documentation/netlinux/netlinux.html

ChangeLog-2.5.45

...dummy **read** check into the **read** ... c In 2.5.44 it **contains** only two ... [IPV4]: Rework key route **lookup** interface ... [SCSI] fix **memory** etc. leak....

From:www.kernel.org/pub/linux/kernel/v2.5/ChangeLog-2.5.45

FAQ: Network Intrusion Detection Systems

...take apart the system and remove the disk drive (and **read/write** it on ... must first **read** the file into **memory** ... The intruder will do a 'whois'

From:www.robertgraham.com/pubs/network-intrusion-detection.html

Untitled

...that stored in database without using a **lookup table**. ... allows you to **read** and **write** virtually any ... TMemoryTable implements BDE in-**memory**...

From:delphi.stts.edu/ftp/d10free/rxlib250.txt

AidAim Software

It **contains** two ... indexes, shareable in **memory** ... It supports calculated and **lookup** fields. ... - **Read** and **write** any portion of data at any file.....

From:delphi.icm.edu.pl/authors/a0003682.htm

ReiserFS

If you **write** 100 byte ... References Also **Read** ... due to the **memory** bandwidth ... directory at a time **lookup** accomplishes a ... which formatted node...

From:www.namesys.com/

BYTE.com

...frequently updated, they reside in an area of **memory** with **read/write** access. ... patching the trap **table**--to function. While the **lookup-table**...

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